REMARKS/ARGUMENTS

Reconsideration of the rejections set forth in the Final Office Action dated June 4, 2004 is respectfully requested. Claims 1-48 are pending in this application. Claims 12 and 34 have been amended to be rewritten in independent form.

Rejections under 35 U.S.C. § 103

The Examiner has rejected claims 1-4, 7-11, 13, 15-17, 18, 22, 35, and 36 under 35 U.S.C. § 103(a) as being anticipated by Smith (U.S. Patent No. 6,188,686) in view of Laor et al. (U.S. Patent No. 6,424,649). The Examiner has rejected claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Smith (U.S. Patent No. 6,188,686) in view of Laor et al. (U.S. Patent No. 6,424,649) further in view of Demiray et al. (U.S. Patent No. 5,740,157). Claim 6 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Lamarche et al. (U.S. Patent No. 6,414,953). Claims 12, 14, 20, 21, 23, and 24 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Tarridec et al. (U.S. Patent No. 4,751,699). Claim 19 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Upp et al. (U.S. Patent No. 5,967,405). Claims 25-34 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Kosugi et al. (U.S. Patent No. 5,189,410). Claims 37, 40-45, 47, and 48 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Madonna (U.S. Patent No. 5,737,320). Claims 38, 39, and 46 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Madonna in further view of Lamarche et al.

1. Independent claim 12 and its dependent

Independent claim 12 requires an apparatus which includes a plurality of interface cards, a cross-connect unit, a control unit, and a backplane forming parallel data buses. The parallel

data buses include a clock recovered parallel data bus that provides connectivity between each of a plurality of interface cards, the cross-connect unit, and the control unit. Data streams are transmitted between the plurality of interface cards and the cross-connect unit over the clock recovered parallel data bus without synchronization information. The clock recovered parallel data bus is a 32-bit clock recovered parallel data bus.

Although the Examiner has argued that Smith in view of Laor et al. and further in view of Tarridec et al. teaches the limitations of claim 12, the Applicants respectfully disagree. On page 6 of the Final Office Action dated June 4, 2004, the Examiner has stated that Tarridec et al. discloses using 32-bit messages in a system that includes clock recovery using a phase locked loop and an oscillator. Contrary to the Examiner's assertions, there appears to be no teaching of using 32-bit messages in Tarridec et al. in the passage cited by the Examiner (column 8 at lines 33-58). Further, there appears to be no teaching of or remote suggestion of a 32-bit clock recovered parallel data bus. While Tarridec et al. does appear to teach of a buffer with a capacity of 32 one-bit cells (Tarridec et al., column 11 at lines 55-63), a buffer with a capacity of 32 one-bit cells is not the same as, and does not suggest, a 32-bit clock recovered parallel data bus. Therefore, claim 12 and its dependent are believed to be allowable over the cited art for at least this reason.

2. Independent claim 34

Among other limitations, independent claim 34 recites an apparatus which includes interface cards that support different STS rates where STS-48 data streams are transmitted over four 4-bit clocked data buses in parallel to each other and STS-12 data streams are transmitted over a single 4-bit clocked data bus. The Examiner has argued that the cited art, taken in combination, teach of such a limitation. The Examiner's specific argument is that "STS rates can be chosen arbitrarily... the oscillator speed can be chosen so that the line will be properly clock recovered" (page 8 of the Final Office Action dated June 4, 2004). The Applicants respectfully submit that the Examiner has failed to address the limitation that STS-48 data streams are transmitted over four 4-bit clocked data buses, while STS-12 data streams are transmitted over a

single 4-bit clocked data bus. Since the Applicants are unable to find any teaching of, or suggestion of, such a limitation in the cited art, claim 34 is believed to be allowable for at least this reason.

It is noted that claims 30-32 also recite limitations pertaining to the number of bits in clocked data buses, which the Examiner does not appear to address in his rejections.

3. Independent claim 35 and its dependent

Independent claim 35 requires that an apparatus includes a plurality of clock recoverable interface cards for transmitting and receiving data streams having no synchronization information and a plurality of clocked interface cards for transmitting and receiving data streams including data and synchronization information. The apparatus also includes a backplane forming parallel data buses including clock recovered parallel data buses and clocked parallel buses that provide connectivity between the interface cards, a cross-connect unit, and a control unit.

In the Final Office Action dated June 4, 2004, the Examiner has admitted that Smith in combination with Laor et al. do not teach or show an apparatus with a plurality of clock recoverable interface cards for transmitting and receiving data streams having no synchronization information and a plurality of clocked interface cards for transmitting and receiving data streams including data and synchronization information. However, the Examiner has argued that the use of both a clock recovered bus and a clocked bus is obvious to one of ordinary skill in the art, because one type of bus could act as a backup for the other bus in case of a failure. The Applicants respectfully submit that the use of both clock recoverable interface cards and clocked interface cards in an apparatus is not obvious, and further submit that in order to provide backup as argued by the Examiner, all data streams apparently must be transmitted both with synchronization information and without synchronization information. Transmitting all data streams both with synchronization information and without synchronization information is not motivated by the cited art, and would not be obvious, as alleged by the Examiner. Accordingly, since claim 35 requires the use of both clock recoverable interface cards and clocked interface cards, claim 35 and its dependent are believed to be allowable over the art of record for at least this reason.

4. Independent claims 37 and 45 and their respective dependents

With regards to claim 37, the Examiner has argued that Smith in view of Laor et al. further in view of Madonna teaches the claimed limitations. It is respectfully submitted that Smith in view of Laor et al. does not teach of signals or payloads which do not include synchronization information, and does not teach of a clock recovered parallel data bus or of transmitting signals over a clock recovered parallel data bus. Madonna also does not appear to teach of payloads which do not include synchronization information, or of a clock recovered parallel data bus. As such, claim 37 is believed to be allowable over the art of record for at least these reasons.

Madonna appears to teach of sending an empty packet from a first node to a second node, and inserting local circuit switched data pertaining to the second node into the empty packet (Madonna, column 14, lines 13-54). Madonna also appears to teach of sending a full packet, full of information pertaining to a first node, from the first node to a second node, and extracting data from the payload at the second node (Madonna, from column 14 at line 55 to column 15 at line 7). On page 11 of the Final Office Action dated June 4, 2004, the Examiner has argued that information extracted from a full packet may subsequently be placed into an empty packet, and that information in a first packet may be processed by a first node before being sent to a second node. The Examiner has also stated that claim 37 only mentions that a second payload includes at least a first telecommunications signal, but that this leaves open the possibility that other information along with the information found in the first packet can be put into the payload of the second packet. It is not clear to the Applicants why the Examiner believes this somehow teaches the claimed invention.

Madonna teaches that the information extracted from a full packet is information associated with an originating node (Madonna, column 14, lines 62-64), and the information placed into an empty packet pertains to a receiving node (Madonna, column 14, lines 29-32). Since Madonna appears to teach that a first node, when sending a full packet, includes only information relating to the first node (in the packet) and also appears to teach that a second node,

when receiving an empty packet, only places information relating to the second node in the packet, in the system of Madonna, information extracted from the full packet by the second node does **not** pertain to the second node and, hence will not be written by the second node into an empty packet. **There is no suggestion in Madonna of a receiving node extracting information associated with the receiving node from a first packet. Also, Madonna teaches that a receiving node places only information pertaining to the receiving node into a second packet, and does not teach of placing any information from an originating node into the second packet.** As such, the Applicants respectfully submit that no combination of Smith, Laor et al., or Madonna teaches of removing a first telecommunications signal from a first payload and inserting the first telecommunications signal in a second payload before transmitting the second payload. Therefore, claim 37 is believed to be allowable over the cited art.

Claims 38-44 each depend either directly or indirectly from independent claim 37 and are, hence, each believed to be allowable over the cited art for at least the reasons set forth above with respect to claim 37.

Independent claim 45 recites similar limitations to those recited in claim 37. Therefore, claim 45 and its dependents are each believed to be allowable over the cited art for at least the reasons set forth above with respect to claim 37.

5. Independent claim 1 and its dependents

Independent claim 1 requires an apparatus which includes a plurality of interface cards, a cross-connect unit, a control unit, and a backplane forming parallel data buses. The parallel data buses include a clock recovered parallel data bus that provides connectivity between each of a plurality of interface cards, the cross-connect unit, and the control unit. Data streams are transmitted between the plurality of interface cards and the cross-connect unit over the clock recovered parallel data bus without synchronization information.

In his rejections, the Examiner has stated that Smith in view of Laor et al. discloses the apparatus as claimed in claim 1. The Applicants respectfully submit that neither Smith nor Laor

et al. alone or in combination, appear to teach of a clock recovered parallel data bus or of transmitting data streams without synchronization information. In the Office Action dated December 31, 2003, the Examiner has acknowledged that Smith does not expressly disclose a clock recovered bus without synchronization information, but argues that "Laor et al. disclosers a switch that operates asynchronously, but appears to operate synchronously by using a single clock signal source which is uniform for the switch interconnect...." (Office Action dated December 31, 2003, page 3). The Examiner further argues that Laor et al. teach of a phase locked loop used for synchronization purposes so that synchronization information does not have to be sent in packets.

The Applicants respectfully disagree with the Examiner's arguments. While Laor et al. appears to teach that a phase locked loop synchronizes to a single frequency source (Laor et al., column 1, lines 61-67), as noted by the Examiner, a phase locked loop that synchronizes to a single frequency source does not show or reasonably suggest that data streams are sent over a clocked recovered parallel data bus without synchronization information. The phase locked loop of Laor et al. does not appear to be a clock recovered data bus, and there is no suggestion in Laor et al. that data steams are sent without synchronization information. Since claim 1 requires a clock recovered data bus, claim 1 is believed to be allowable over the art of record for at least this reason.

It is submitted that a phase locked loop as taught by Laor et al. which synchronizes to a single frequency source does not imply that phase locked loops are used so that synchronization information does not have to be sent, as alleged by the Examiner. There appears to be no suggestion of not sending synchronization information in Laor et al. Even if it is assumed that a phase locked loop does not use any synchronization information from data to synchronize, there is still no teaching or suggestion in Laor et al. that synchronization information is not included in a data stream. The information may still be included in the data stream, since Laor et al. does not teach or suggest that the information is not included in the data stream. As Laor et al. does not appear to teach of, or even suggest, sending data streams without synchronization information, claim 1 is also believed to be allowable over the art of record for at least this reason as well.

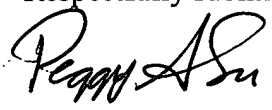
Claims 2-11 and 13-33 each depend either directly or indirectly from independent claim

1, and are therefore each believed to be allowable over the art of record for at least the reasons set forth above with respect to independent claim 1. Each of these independent claims recites additional limitations which, when considered in view of claim 1, are believed to further distinguish the claimed invention over the art of record. By way of example, it is noted that the Examiner has apparently changed his rejection of claim 18, and acknowledged that the cited art does not teach of the limitations of claim 18. However, the Examiner has argued that "grouping a first set of ports together into one telecommunications plane while grouping a second set of interfaces together into a second data plane" would be obvious to a person of ordinary skill in the art (Office Action dated June 4, 2004, page 4). It is respectfully submitted that contrary to the Examiner's assertions, the grouping of interface subsystems into a telecommunications plane and a data plane is not obvious, as there is no teaching or motivation in the cited art to even consider the grouping of interface cards into subsystems. Therefore, claim 18 is believed to be allowable over the cited art for at least this reason as well.

Conclusion

For the foregoing reasons, Applicant believes all the pending claims are in condition for allowance and should be passed to issue. If the Examiner feels that a telephone conference would in any way expedite the prosecution of the application, please do not hesitate to call the undersigned at (408) 446-8696.

Respectfully submitted,



Peggy A. Su
Registration No. 41,336

RITTER, LANG & KAPLAN LLP
12930 Saratoga Ave., Suite D1
Saratoga, CA 95070
Tel: (408) 446-8696
Fax: 408-446-8691
PAS/acc